CLAIMS

1. A phase-locked loop including:

an oscillator, controlled by a control signal generated by a comparison circuit comparing a reference frequency with an oscillator frequency and filtered by an integrator low-pass filter;

a control and adjustment circuit for, with a predetermined frequency smaller than the reference frequency, taking into account the value of the filtered controlled signal and, if this value is out of a range of predetermined values, adjusting the operating range of the oscillator; and

an inhibition circuit for deactivating the comparison circuit for a predetermined duration before taking into account the value of the filtered control signal.

2. The phase-locked loop of claim 1, wherein the inhibition circuit is activated only if the value of the filtered control signal is out of the range of predetermined values.

3. The phase-locked loop of claim 1, wherein the oscillator, the comparison circuit, the control and adjustment circuit, and the inhibition circuit are made in an integrated circuit.

4. The phase-locked loop of claim 1, wherein the filter includes a first capacitor connected in series with a first resistor between an input/output terminal and a ground, a second capacitor, of small capacitance as compared to the first capacitor, being connected between the input/output terminal and the ground.

5. The phase-locked loop of claim 1, wherein the comparison circuit includes first and second D flip-flops respectively rated at the reference frequency and at a variable frequency equal to a predetermined ratio of the oscillator frequency, the input terminals of the D flip-flops being connected to 1, the output terminal of the first flip-flop generating an incrementation signal, the output terminal of the second flip-flop generating a decrementation signal, a reset terminal of the D flip-flops being activable by

a NAND combination of the incrementation and decrementation signals, the output terminal of the comparison circuit being connected via a first switch to a source of a positive constant current, the first switch being respectively on or off when the incrementation signal is at 1 or 0, the output terminal of the comparison circuit being further connected via a second switch to a source of a negative constant current, the second switch being respectively on or off when the decrementation signal is at 1 or at 0.

6. The phase-locked loop of claim 5, wherein the oscillator includes an amplifier with a negative resistance, the output of which is the oscillator output, the input of the amplifier being connected to a first terminal of a third capacitor, the second terminal of the third capacitor being connected to the oscillator input via a second resistor, a varicap diode being connected by its cathode to the second terminal of the third capacitor, the anode of the varicap diode being connected to ground, an inductance and a variable capacitor being connected in parallel between the input of the amplifier and the ground, the capacitance of the variable capacitor being controlled by an adjustment signal.

7. The phase-locked loop of claim 6, wherein the control and adjustment circuit includes a first comparator enabling comparison of the filtered control signal with a high predetermined voltage, a second comparator enabling comparison of the filtered control signal with a low predetermined voltage, the first and second comparators controlling a coding block which controls via an adder the incrementation or the decrementation of the adjustment signal, stored in a third D flip-flop clocked at said predetermined frequency by a clock signal.

8. The phase-locked loop of claim 7, wherein the inhibition circuit includes a fourth D flip-flop generating an inhibition signal, the fourth flip-flop being clocked by the inverse of the clock signal and reset by the high state of the clock signal, the input terminal of the fourth D flip-flop receiving a signal equal to 1 when the control signal is greater than the high predetermined voltage or smaller than the low predetermined

voltage, and equal to 0 otherwise, and two AND gates arranged to cancel the incrementation and decrementation signals respectively provided by the first and second D flip-flops to the first and second switches when the inhibition signal is equal to 1.

9. A method for controlling a phase-locked loop including an oscillator controlled by a control signal generated by a comparison circuit comparing a reference frequency with the oscillator frequency and filtered by an integrator low-pass filter, including the steps of:

taking into account the value of the filtered control signal with a predetermined frequency smaller than the reference frequency and adjusting the operating range of the oscillator if the value of the filtered control signal is out of a range of predetermined values; and

deactivating the comparison circuit during a predetermined duration before taking into account the value of the filtered control signal.